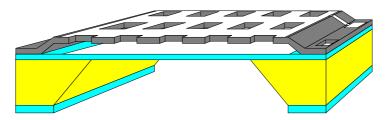
# Realisation of a **micromechanical microphone**

with frontside contacts

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# **Summary**

The microphones made so far, all need an electrical concact on the backside of the substrate. If a microphone is to be integrated with true CMOS electronics, it is required that the silicon substrate is electrically grounded. This introduces serious insulation problems between the backplate electrode and the substrate. Furthermore, the electrode on the back has to be connected with low parasitic capacitance to the electronics on the front.

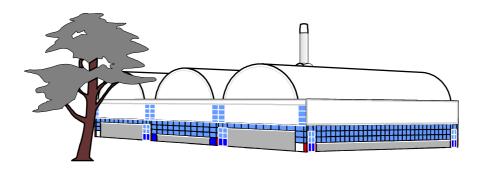
In this report an adaption to the conventional microphone of Patrick Scheeper that results in a microphone with two frontside contacts is described. It was found that skipping from gold to chrome conductors the silicon process becomes less critical.

The condenser microphone actually is a parallel plate capacitor with one plate perforated. For the perforated capacitor there were no accurate models available to calculate the static capacitance. Two methods to get an impression are given here. The first uses the theory of conformal mapping by which a known structure is being transformed to the unknown structure. From the transformation information can be obtained about the capacitance.

A second method was necessary because conformal mapping only gives a two dimensional image. This second method was an iterative method by which the desired charge distribution is obtained from which the capactiance can be calculated. This method was verified but not applied on the microphone.

To qualify the microphone after processing the static capacitance was used. Because the devices are located on a wafer this capacitance must be measured with probes. The probes will introduce capacitances and the actual value will not be clear. In this project the capacitor was placed in an active shielded RC-network from which the capacitance was calculated.

The microphones were realised in the MESA cleanroom laboratory.



## **Preface**

The assignment to adapt an existing microphone was a multi experience task. The realisation was done using the interesting cleanroom science, the modelling required a study of fundamental math methods and the building of the measurement set-up was impossible without knowing something about electronics.

With this preface I like to thank Michael Pedersen for supporting the development of the project. Special thanks goes to Johan Bomer who did the process steps I was not allowed to and Dion Oudejans who tried to replace Johan when he was on vacation. Henri Jansen for having some interesting technology tips and Huib van Vossen for giving the cleanroom courses.

The people that I do not mention with their names are the rest of the exam committee and some members of the cleanroom staff.

Geert Langereis, September 1994

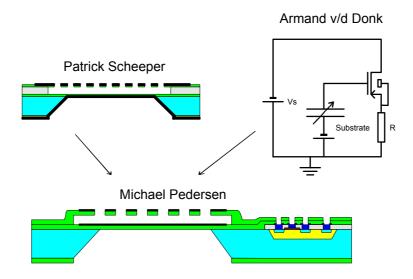
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# 1. About the project

In this chapter a description is given about the project and the research items from which it has been formulated.

The first Ph.D. work on the silicon microphone was Armand van der Donk [1]. He did some research on the modelling of the microphone and on the electrical supplies. During his work a second scientist was appointed. This was Patrick Scheeper [2] who took part of the design and realisation of the actual device.



11 The work of three Ph.D. projects on the silicon microphone project

A logical completion is the integration of the micromechanical structure with the supporting electronics. This is currently done by Michael Pedersen. The history is schematically visualised in figure 1.1.

During this integration some problems occur. The microphone is not yet compatible with the process steps necessary to realise the electronics with a CMOS process. Also some practical problems prevent a simple integration. One of them is that the microphone as developed by Patrick Scheeper has one contact on the upper side and one on the backside. This electrically claims the bulk material which must be grounded using CMOS technology. At the same time the connection to the backside contact of the electronics is hard to make.

This was the reason that a student assignment was formulated to support the graduating project. The aim of the assignment was the development of a microphone with two contacts on the frontside.

# 2. Introduction

In this chapter some general information is summarised about silicon microphones and the electronics required to optimise operation. Because this project is merely focused on process technology there is not much attention paid to the characteristics of the microphone. The microphone and the process of Patrick Scheeper [2] are taken as the starting point for designing a structure with only front sided contacts that is easier to integrate with the MOS-technology.

## 2.1. The condenser microphone

The principle of the condenser microphone is based on the fact that the voltage across a capacitor is dependent on the capacitance:

$$u = \frac{q}{C}$$

Where:

u: the voltage across the capacitor

q: the stored charge on the capacitor

C: the capacitance

The capacitance for a parallel plate capacitor is dependent on the surface A of the plates, the plate distance x and the dielectric constant of the airgap  $\varepsilon_0$ :

$$C = \frac{\varepsilon_0 A}{x}$$
 2.2

For a parallel plate capacitor with one movable plate the following transduction equation can be formulated:

$$du = \frac{x_0}{\varepsilon_0 A} \cdot dq + \frac{q_0}{\varepsilon_0 A} \cdot dx$$

$$dF = \frac{q_0}{\varepsilon_0 A} \cdot dq + D \cdot dx$$
2.3

With:

 $x_0$ : the distance between the plates if no pressure is applied

 $\varepsilon_0$ : the dielectric constant

A: the area of the plates

 $q_0$ : the stored charge at rest

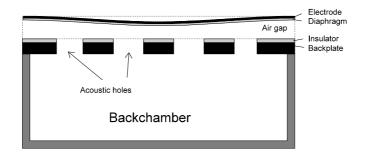
x : the distance between the plates

F: the force applied on the moving plate

D: the spring constant of the moving plate

It is clear that a transduction only takes place if  $q_0 > 0$ , only then a fluctuation in the plate distance x causes a change in the electrical measurable parameters. This means that the condenser microphone must be biased to produce a signal.

A schematic representation of a condenser microphone is given in figure 2.1.

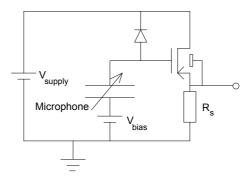


21 Structure of the condenser microphone

With this structure the spring which causes the constant D in equation 2.3 is formed by the stiffness of the diaphragm. The backchamber garantees a pressure gradient across the plate.

It was mentioned that for electro-mechanical transduction a bias voltage is necessary. The microphone will be used in a hearing aid using a small battery. This means that the required bias voltage is not available, so this relatively high voltage must be generated from the available battery. To do this a voltage multiplier will be needed.

Besides the voltage multiplier a pre-amplifier is needed. The purpose is to integrate this pre-amplifier on one chip with the microphone and the multiplier to reduce noise and the capacitive loading of the microphone.



22 Electrical circuit of microphone and pre -amplifier

In figure 2.2 the microphone is represented by the large variable capacitor. The pre amplifier consists of a single MOS transistor, a resistor  $R_s$  and a diode. This amplifier is supplied by  $V_{supply}$ . The bias voltage is represented by the source  $V_{bias}$ .

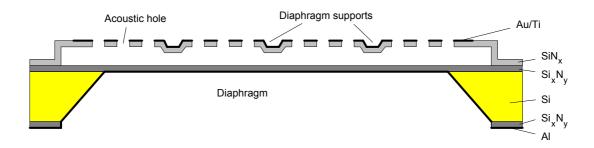
#### 2.2. The conventional silicon microphone process

The microphone that is the base of the one that has been developed can be found in the publication of Patrick Scheeper [2].

The structure of this microphone is drawn in figure 2.3. It is a sacrificial-two sided one and consists of the following steps:

- LPCVD Si<sub>x</sub>N<sub>v</sub> deposition on both sides.
- RIE-etch of nitride on back side (mask 1).

- Partial KOH-etch of silicon from backside.
- Evaporation of aluminium on front side (for sacrificial layer).
- Phosphoric acid etch of diaphragm supports on front side (mask 2).
- Phosphoric acid etch to define sacrificial layer area (mask 1 again).
- PECVD SiN<sub>x</sub> deposition on front side.
- Titanium and gold deposition on front.
- Etching of gold and RIE-etch of nitride for acoustic holes (mask 3).
- Complete KOH-etch of silicon on backside.
- Sacrificial layer etch with phosphoric acid (using mask 4).
- Freeze drying.
- Evaporation of Al on backside.



23 Conventional silicon microphone

The result is a four mask process by which a microphone with one back-side and one front-side contact is defined. The back-side contact becomes a problem when the microphone is combined with the electronics because the CMOS technology uses a grounded bulk. As it already has been said, the aim of this project is to adapt the process to obtain two front-side contacts.

Because the spring constant of the diaphragm is formed by the deflection of the structure, the material used is very critical. Patrick Scheeper matched the process to obtain a low tension which results in the desired spring constant [2]. These parameters will be reused in the new process.

## 2.3. Demands on the new process

A logical result of the work of Armand van der Donk [1] and Patrick Scheeper [2] is the project of Michael Pedersen. His aim is to combine the MOS-technology with the silicon micromechanical microphone on one chip. The two technologies are quite different, this is the reason that the ICE (MOS electronics) and the S&A (sensors and actuators) parts are separated in the MESA laboratory. Because of the strong demands on the MOS technology one is not allowed to bring the microphone in the ICE machines, so first the electronics must be processed before applying the microphone. This has its consequences on the production method.

The new process is restricted by the following points:

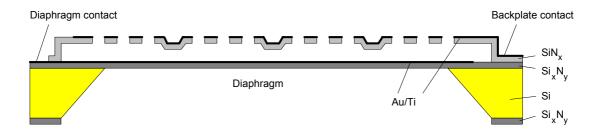
• The micromechanical steps must be MOS-compatible. It is not allowed to destroy the possible present electronic components. This will lead to the restriction of a

maximal allowable temperature of 300°C. There are probably some more unknown influences of processing steps.

- No extra parasitic capacitances may be introduced.
- The sacrificial layer etching should be one of the last processing steps, so the connections to the conductive material on the diaphragm should be ready before this step of the process.
- There are now three masks used (one for the back-side and two for the front side). It is not convenient to increase this number too much.

# 2.4. First idea of making the contact

Assuming that moving the conductive layer on the diaphragm from the back-side to the front side gives no important differences in the characteristics of the microphone the following structure is an option for a microphone with two front-side contacts.



24 Microphone with two front-side contacts

Processing this microphone requires one more mask and some steps to define the diaphragm conductor. To check the presence of the new conductor the static capacitance may be used. In the next chapter a description will be given of a method to measure the capacitance of the microphone. This capacitance gives an indication of the size of the air gap, the quality of the conductors and the series resistance.

# 3. The static microphone capacitance

Finding the static capacitance of the microphone is not an easy job. Although a dual parallel plate capacitor is easy to solve, the microphone with a perforated backplate is much more difficult. First the capacitance is analytically evaluated by using a mathematical transformation known as "conformal mapping". Another option is to find the charge distribution by solving Laplace's equation numerically. This method is used in the second section.

## 3.1. The ideal capacitor

Formula 2.2 gave the capacitance for an ideal square parallel plated capacitor:

$$C = \frac{\varepsilon_0 A}{x}$$
 22

This formula is does not implement boundary effects and is for gaps without dielectric fill. Figure 2.4 showed however that the backplate material will be in between the conducting plates. For a partially filled air gap the capacitance becomes the series equivalent of the two partial capacitors:

$$\begin{split} C_{tot} &= C_{air} /\!/ C_{diel} = \left( \left( \frac{\epsilon_0 A}{d_{air}} \right)^{-1} + \left( \frac{\epsilon_0 \epsilon_r A}{d_{diel}} \right)^{-1} \right)^{-1} \\ C_{tot} &= \frac{\epsilon_0 A}{d_{air} + \frac{d_{diel}}{\epsilon_r}} \end{split}$$
 3.1

Where  $d_{air}$  is the thickness of the air gap and  $d_{diel}$  is the thickness of the dielectric fill. Note that  $x = d_{air} + d_{diel}$ . For silicon nitride which is the material that will be in the air gap the relative dielectric constant is  $\epsilon_r = 4.2$  [4]. In the realisations the air gap is 3  $\mu$ m, the thickness of the silicon nitride backplate is 1  $\mu$ m and the sizes of the microphones are between 1.5×1.5 mm and 2.5×2.5 mm. The next table shows some calculations using equation 3.1:

Table 3.1: Some theoretical capacitances

Size [mm <sup>2</sup> ]	C [pF]	Cstick [pF]
1.5×1.5	6.1	83.6
2.0×2.0	10.9	148.7
2.5×2.5	17.1	232.3

The third column shows the capacitance if the air gap is zero over the complete area A) for example due to the phenomenon called 'sticking' which is evaluated in a following chapter. This makes it clear that by measuring the static capacitance we are able to say something about the condition of the microphone.

## 3.2. Analytical two dimensional solution

The electric potential distribution of a system of conducting structures (as capacitors are) is the solution of Laplace's equation [5]:

$$\nabla^2 \mathbf{V} = 0 \tag{32}$$

This formula describes the potential in a simple medium where there is no free charge. If the potential distribution is known, the electric field can be determined by:

$$\mathbf{E} = -\nabla \mathbf{V} \tag{33}$$

From the electrical field the charge distribution in the (surface of the) conductor can be found by using Gauss's law. This law gives the boundary conditions at the interface of a conductor and free space. The normal component of the electric field  $E_{\perp}$  is proportional to the surface charge density  $\rho_s$ :

$$\mathbf{E}_{\perp} = 0$$

$$\mathbf{E}_{\perp} = \frac{\rho_{s}}{\varepsilon_{0}}$$
34

Laplace's equation 3.2 can be very difficult to solve. One method to find the potential distribution is the way of separation of variables [5] but this can not be simply used in this case. A more promising solution method is the conformal mapping evaluated in the next section.

## 3.2.1. The method of conformal mapping

"Mapping" is the geometric transformation of one plane to another. Laplace's equation is still valid in the mapped plane if the transformation is "conform", which means that curves which intersect at right angles in the original plane continue to do so on the other plane. The aim of the conformal mapping is to map a configuration with a known solution of Laplace's equation to the structure to be solved. The conformal mapping will transform the potential distribution in the known plane to the unique solution in the mapped plane.

The transformation formula's will be complex analytical functions [6]. Because, if u(x,y) is a solution of Laplace's equation (is a harmonic function), a unique complex conjucated function v(x,y) exists with

$$f(x,y) = u(x,y) + i \cdot v(x,y)$$
35

is complex analytical. The function f(x,y) is the transformation formula.

As an example the field of a finite plate capacitor is derived [7]. This transformation which goes from an infinite plate capacitor to the desired structure can be explained by two successive steps. Let us first examine the function

$$z = e^{w}$$

Both w and z are complex numbers with

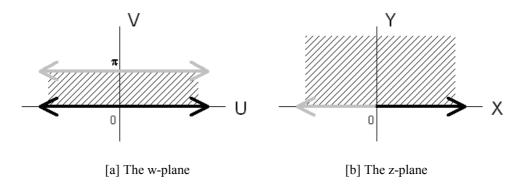
$$z = x + iy$$

$$w = u + iy$$
37

So function 3.6 is an implementation of f(x,y). We can calculate the following points:

X	у		u	V
- ∞	π	$\Rightarrow$	0	0
- ∞	0	$\Rightarrow$	0	0
$\infty$	0	$\Rightarrow$	$\infty$	0
$\infty$	π	$\Rightarrow$	- ∞	0
0	π	$\Rightarrow$	- 1	0

Graphically the transformation of the lines w(u,v) = u and  $w(u,v) = u + i\pi$  can be viewed as:



31 Transformation  $z = e^{w}$ 

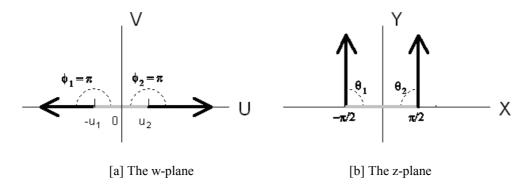
It can now be concluded that function 3.6 is the conformal transformation of an infinite dual plate capacitor to the structure of figure 3.1b. The upper plate of figure a is mapped to the negative real axis of figure b, the lower plate is mapped to the positive real axis. Now the field of the dual plate can be analytically solved and then be transformed to the field that must be the solution of Laplace's equation for figure 31b.

This transformation is the first of the two steps required to solve the finite parallel plate capacitor. The second step transformes figure 3.1b to the desired configuration. This second step is used here to explain the importance of the Schwarz-Christoffel equation.

Finding the transformation formula can be very difficult. One way to find a transformation is solving the Schwarz-Christoffel formula:

$$z = K \int (w - u_1)^{\frac{\theta_1}{\pi} - 1} (w - u_2)^{\frac{\theta_2}{\pi} - 1} dw + C$$
 38

The derivation of this integral is given in the book of Nussbaum [7]. The Schwarz-Christoffel transformation gives the relation between a structure with angles  $\theta_1$  and  $\theta_2$  in the z-plane and a structure with angles  $\pi$  at  $u = u_1$  and  $u = u_2$  in the w-plane (figure 32). From the boundary conditions we must find the constants C and K.

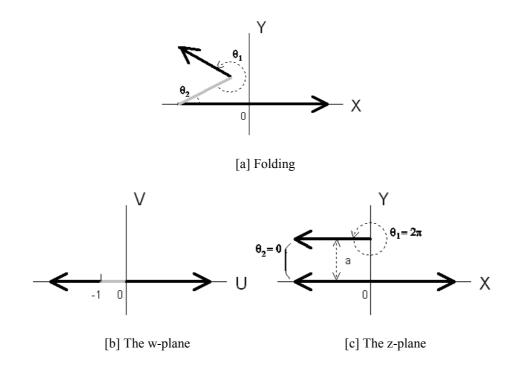


32 The Schwarz -Christoffel transformation

Starting with figure 3.1b as being the w-plane of figure 3.2, take

$$\begin{array}{ll} u_1=-1 & \theta_1=2\pi \\ u_2=0 & \theta_2=0 \end{array} \label{eq:theta_1}$$
 39

as parameters. The transformation becomes like figure 3.3.



33 Application of the Schwarz-Christoffel transformation

Equation 3.8 can be solved using the boundary conditions  $K = a/\pi$  and  $C = a/\pi$ :

$$z(w) = \frac{a}{\pi}(w + \ln w + 1)$$
 310

This is the second step in solving the finite capacitor. Using equation 3.6, the complete transformation which converts the parallel plate capacitor to the structure of figure 3.3c has been found. The formula for the potential is the solution for the infinite parallel-plate capacitor having a plate distance  $\pi$ , and is only a function of v = Im w. This potential goes linearly from upper plate potential  $V_0$  to the grounded lower

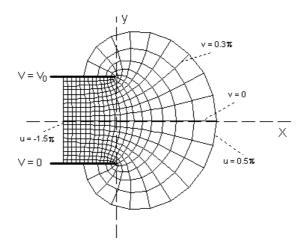
plate:  $V(v) = V_0 \cdot v/x$ . With plate distance  $x = \pi$  and v the imaginary axis in the w plane resulting in  $V(w) = V_0 \cdot Im(w)/\pi$ 

$$z(w) = \frac{a}{\pi} (e^{w} + w + 1)$$

$$V(w) = V_0 \frac{\text{Im } w}{\pi}$$
311

Summarising this equation relates the known potential distribution in the w(u,v) plane to the desired distribution in the z(x,y) = z(w(u,v)) plane. Note that sometimes the word "mapping" is used for the transformation from the "real" world to the equivalent world, and sometimes inversely. The planes z(x,y) and w(u,v) are being used as origin and result of the transformation and do not consequently correspond to one of the two worlds. Hopefully this removes some confusion about the w plane in figure 3.3b which is the same as the z plane in figure 3.1b.

In figure 3.4 the result of equation 3.1 lis plotted. This plot is a parametric plot with u going from  $-1.\pi$  to  $0.5\pi$  (equi-potential lines) and v from  $-\pi$  to  $\pi$  (the electric field lines). Appendix C illustrates the method to draw a plot like this.



34 The complete parallel -plate capacitor

Here another technique is used. If a system of charges is placed in front of a grounded metal plate, we are allowed to mirror the charge while changing the sign, still giving a valid field distribution. This is called the method of images [5] and gives us the complete solution from the single sided version.

#### 3.2.2. Solving the infinite, single perforated capacitor

Let us first examine the function

$$z = -a \cdot \coth \frac{w}{2}$$
 312

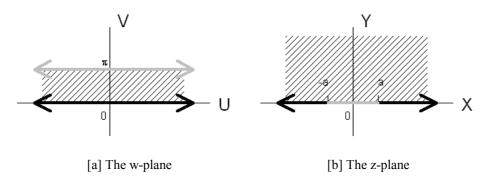
With

$$coth(w) = \frac{e^{2w} + 1}{e^{2w} - 1}$$
313

Both w and z are complex numbers like 3.7. Calculating some points again:

X	у		u	V
- ∞	π	$\Rightarrow$	a	0
~	π	$\Rightarrow$	- a	0
- ∞	0	$\Rightarrow$	a	0
$\infty$	0	$\Rightarrow$	- a	0
0	π	$\Rightarrow$	0	0
- 0	0	$\Rightarrow$	$\infty$	0
+ 0	0	$\Rightarrow$	- ∞	0

Now the transformation of the lines w(u,v) = u and  $w(u,v) = u + i\pi$  can be viewed by:



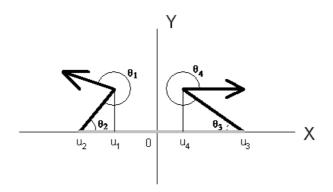
35 Transformation  $z = -a \coth(w/2)$ 

So function 3.12s the conformal transformation of an infinite dual plate capacitor to the structure of figure 3.5b. The upper plate of figure a is mapped to the part between z = -a and z = a of figure b, the lower plate is mapped around this area.

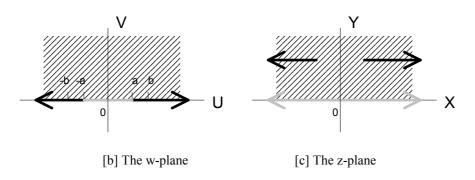
To obtain a capacitor with a hole in the upper plate from figure 3.5b a transformation like figure 3.3 is needed two times, one time on the negative real axis and one time on the positive real axis. So the Schwarz-Christoffel equation which supports two bending points must be adapted to a fourth order version:

$$z = K \int \prod_{i=1}^{4} (w - u_i)^{\frac{\theta_i}{\pi} - 1} dw + C$$
 3.14

Only then the structure of figure 3.6b can lead to figure 3.6c by folding like figure 3.6a.



[a] The constants in the Schwarz-Christoffel equation



36 Illustration of the four points Schwarz -Christoffel transformation

The constants in 3.14are:

$$\begin{array}{lll} u_1 = -b & \theta_1 = 2\pi \\ u_2 = -a & \theta_2 = 0 \\ u_3 = a & \theta_3 = 0 \\ u_4 = b & \theta_4 = 2\pi \end{array} \label{eq:def_u1}$$
 315

The potential of the area between -a and +a in the w-plane is 0 Volt and outside this area  $V_0$  Volt. Equation 3.14becomes:

$$z = K \int (w+b)(w+a)^{-1}(w-a)^{-1}(w-b)dw + C$$

$$z = K \int \frac{(w+b)(w-b)}{(w+a)(w-a)}dw + C$$

$$z = K \int \frac{w^2 - b^2}{w^2 - a^2}dw + C$$

$$z = K \int \frac{w^2 - a^2 + a^2 - b^2}{w^2 - a^2}dw + C$$

$$z = K \int 1 + \frac{a^2 - b^2}{w^2 - a^2}dw + C$$

$$z = K \cdot w + K \int \frac{a^2 - b^2}{w^2 - a^2} dw + C$$

$$z = K \cdot w + K \frac{b^2 - a^2}{a^2} \int \frac{1}{1 - (\frac{w}{a})^2} dw + C$$

The solution of the integral is the hyperbolic arccotangens:

$$\operatorname{arcotgh}(w) = \frac{1}{2} \ln \frac{x+1}{x-1}$$
 316

The integral becomes:

$$z = K \cdot \left[ w + \frac{b^2 - a^2}{2a^2} \ln \frac{\frac{w}{a} + 1}{\frac{w}{a} - 1} \right] + C$$
 3.17

The complete transformation comes from equation 3.17 and 3.12 and is:

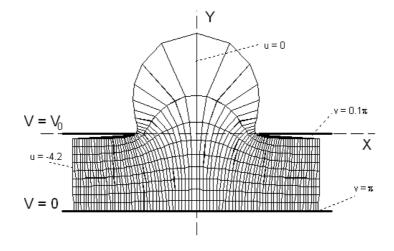
$$z(w) = -K \left[ a \cdot \coth(\frac{w}{2}) + \frac{b^2 - a^2}{2a^2} w \right] + C$$
 3.18

Let's take for example a = 1 and b = 2 then we have

$$z(w) = \frac{2}{3} \cdot \coth(\frac{w}{2}) + w$$

$$V(w) = V_0 \frac{\text{Im } w}{\pi}$$
3.19

Here is used that C = 0 and K = 2/3 to garantee that the plate distance is  $\pi$  as in figure 3.5. We have now solved the field for an infinite dual plate with a hole in the upper plate. The result is plotted in figure 3.7 with field lines from  $v = 0.1\pi$  to  $\pi$  and equipotential lines from  $v = 0.1\pi$  to  $\tau$  and equipotential lines from  $\tau$  and equipotential lines from  $\tau$  and equipotential lines from  $\tau$  and equipotential lines.

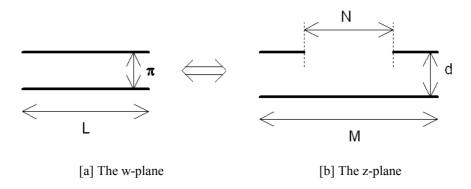


3.7 Field of an infinite capacitor with one hole

From this structure we would like to place a large number next to each other to get the structure of a microphone with a perforated back-plate. In the next section the capacitance of one unit is evaluated by mapping it to a finite dual plate capacitor.

#### 3.2.3. The capacitance of an infinite perforated dual plate

The geometrical parameters of figure 3.7 are now expressed in terms of the parameters of a finite capacitor using equation 3.18The names are illustrated in figure 3. 8.



38 Transformation parameters

First the plate distance in the z plane with K is real is found by:

$$Im(z(\infty)) = -Ka + Im(C)$$

$$Im(z(\infty + i\pi)) = -K \left[ a + \frac{b^2 - a^2}{2a^2} \pi \right] + Im(C)$$

$$d = Im(z(\infty + i\pi)) - Im(z(\infty)) = -K \left[ \frac{b^2 - a^2}{2a^2} \pi \right]$$
3.20

From this it will also be clear that the constant C only gives a shift of the structure of Im(C) in the y-direction. To find the size of the hole we must find which point in the w-plane (called  $u_N$ ) is mapped to the edge of the hole in the z-plane:

$$\frac{d}{du} \operatorname{Re}(z(u_{N})) = -K \frac{d}{du} \left[ a \cdot \coth(\frac{u_{N}}{2}) + \frac{b^{2} - a^{2}}{2a^{2}} u_{N} \right]^{\operatorname{def}} = 0$$

$$-K \left[ a \cdot \frac{-2e^{u_{N}}}{(e^{u_{N}} - 1)^{2}} + \frac{b^{2} - a^{2}}{2a^{2}} \right] = 0$$

$$u_{N} = \ln \left[ \frac{b^{2} - a^{2} + 2a^{3} + 2\sqrt{a^{3}(b^{2} - a^{2} + a^{3})}}{b^{2} - a^{2}} \right]$$

$$3.21$$

$$N = 2 \cdot \operatorname{Re}(z(u_{N})) = 2 \cdot z(u_{N})$$

$$3.22$$

The third condition is that the length M should be the mapped to the length L for both the upper plate as the lower plate:

$$\operatorname{Re}(z(\frac{1}{2}L + i\pi)) = -K \left[ a \cdot \frac{e^{\frac{L}{2}} - 1}{e^{\frac{L}{2}} + 1} + \frac{b^2 - a^2}{4a^2} L \right]^{\operatorname{def}} = \frac{M}{2}$$
 323

$$Re(z(\frac{1}{2}L)) = -K \left[ a \cdot \frac{e^{\frac{L}{2}} + 1}{e^{\frac{L}{2}} - 1} + \frac{b^2 - a^2}{4a^2} L \right]^{\text{def}} = \frac{M}{2}$$
 324

To avoid a contradiction between equations 3.23 and 3. 24 (they are equal exc ept for the signs in the exponential part) we must choose L >> 2 and we find from both:

$$-K\left[a + \frac{b^2 - a^2}{4a^2}L\right]^{\text{def}} \frac{M}{2}$$
 3.25

By scaling of the parameters the condition L >> 2 can be satisfied. The result of calculating M, N and d is that we have three equations defining L, K, a and b. Although b > a we can choose one free (for example a). We are still free to choose the constant C representing the translation in the z-plane and one of the constants a, b, and K. Here is a summary of the model with C = 0:

$$d = -K\pi \left(\frac{b^2 - a^2}{2a^2}\right)$$
 3.20'

$$N = 2 \cdot z(u_N)$$
 3.22'

$$M = -K \cdot \left[ 2a + \frac{b^2 - a^2}{2a^2} \cdot L \right]$$
 3.25'

With:

$$u_{N} = \ln \left[ \frac{b^{2} - a^{2} + 2a^{3} + 2\sqrt{a^{3}(b^{2} - a^{2} + a^{3})}}{b^{2} - a^{2}} \right]$$

We are interested in the a, b, L and K that correspond with the given d, M and N. These must be solved from the equations 3.20', 3.22' and 3.25' where for example a can be set to a constant value that gives a good converging. Appendix D gives an example of solving the system with the mathematical simulation program MathCad.

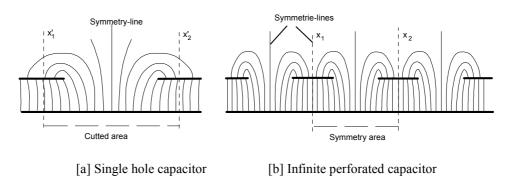
When the constant L is solved, the relation for the equivalent capacitor is the same as 2.2:

$$C_{eq} = \frac{\varepsilon_0 A_{eq}}{X_{eq}} = \frac{\varepsilon_0 \cdot L \cdot L_d}{\pi}$$
3.26

Here is L<sub>d</sub> the depth of the plate (perpendicular to the z-plane) and is for both the original as the mapped structure the same. This value is used to transform from a two dimensional structure to a three dimensional equivalent.

#### 3.2.4. The validity of the solution

The idea of putting an infinite number of single perforated capacitors next to each other is an approximation and should be verified. In the exact solution of an infinite perforated plate two types of symmetry-lines will be present: one in the middle of each hole and one just between two holes (figure 3.9b). It is possible to define a unit going from line  $x_1$  to  $x_2$  that is repeated infinite times.



39 Symmetry lines in structures

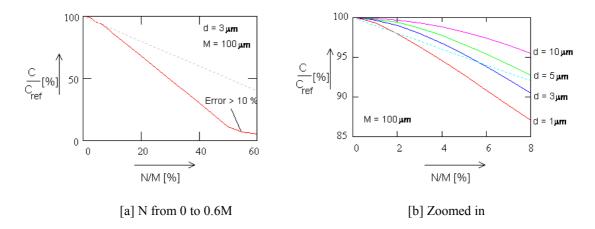
In the solution of the mapping method, the structure of figure 3.9a is derived. We are not able to define a finite area here which can be repeated to obtain figure b. Always some field lines will cross the cutting lines unless they are taken in  $-\infty$  and  $+\infty$ .

In the model we approximate the symmetry-lines at  $x_1$  and  $x_2$  with cutting lines at  $x_1$ ' and  $x_2$ '. The distance between  $x_1$ ' and  $x_2$ ' will be the length L used in the previous section. (Notice that with the ideal infinite plate capacitor the cutting region is always a symmetry region because the field lines are parallel everywhere.)

As a value for the accuracy of the cutting the linearity of the inner plate field lines at the cutting lines can be used. With the structure of figure 3.9b these lines would be straight. If the mapped ideal parallel plate capacitor is cut at  $Re(w) = u_1$  the error in the perforated model will be:

Error = 
$$\left(1 - \frac{\operatorname{Re}(z(u_1 + i\pi))}{\operatorname{Re}(z(u_1))}\right) \cdot 100\%$$
 3.27

With the method of Appendix D the capacitance was calculated for a capacitor with gap 3  $\mu$ m, a length of 100  $\mu$ m and a hole size going from 0 to 100  $\mu$ m.



31(Relative capacitance with changing hole size

In figure 3.10 N was varied fr om 0 (no hole) to 0.6M (more than 50 % hole). The capacitance is normalised to the capacitor without a hole, so at N=0 we find a capacitance of 100%. As a reference the line for a capacitor with no fringing effects is used: decreasing in a straight line from 100% at N=0 to 0 % at N=M.

With holes bigger than 0.5 times N the error became 1%, at 0.55 times N the error was 10%. So the model is reliable up to hole ratio's of about 50%.

From figure 3.10 it is clear that for small holes the capacitance does not change a lot: the lines are allmost horizontal for very small holes. This could be expected because the field lines will bend so that at the (not perforated) bottom plate the presence of this hole can hardly be measured. This effect is stronger with larger air gaps.

For large hole ratios the capacitance changes faster than with an ideal capacitor because now the field line density on the bottom plate becomes relatively lower.

The disadvantage of the result is that it gives a two dimensional solution for an infinite structure. The holes in the two dimensional case are actually infinite grooves in the three dimensional case. The conformal mapping can not be applied for three dimensions because it uses the complex plane which is restricted to the real and imaginary axis.

Because we are interested in a finite three dimensional configuration another method is evaluated in the following section.

#### 3.3. Simulating a three dimensional structure

A numerical method was evaluated by Fred Dijkstra as a 100 hours assignment [8]. His method was based on the equation:

$$V = \frac{1}{4\pi\varepsilon_0} \sum_{k=1}^{n} \frac{q_k}{R_k}$$
 3.28

which is a solution of 3.3 and states that the potential at a certain point is equal to the sum of all electrical field components caused by the charges  $q_k$  at distance  $R_k$ . For a parallel plate with  $n \times n$  partitions a matrix equation giving the potential at each point is given by:

$$\begin{bmatrix} V_{1} \\ \cdot \\ V_{n^{2}} \end{bmatrix} = \frac{1}{4\pi\epsilon_{0}} \begin{bmatrix} \frac{1}{R_{11}} & \cdot & \frac{1}{R_{n^{2}1}} \\ \cdot & \cdot & \cdot \\ \frac{1}{R_{1n^{2}}} & \cdot & \frac{1}{R_{n^{2}n^{2}}} \end{bmatrix} \cdot \begin{bmatrix} q_{1} \\ \cdot \\ q_{n^{2}} \end{bmatrix}$$
329

It is known that the potential in a conducting plate is equal so  $V = V_i$  for every i. From this matrix equation the charge distribution  $q_i$  can be solved using either Gauss elimination, Kramer's rule or LU-decomposition. Note that for a partition of  $n \times n$  a  $n^2 \times n^2$  matrix must be solved, this is for two plates a matrix with  $4 \times n^2 \times n^2$  components. If n = 100 the matrix needs 400.000.000 elements, if the data type is a real (6 bytes) the storage requires 2.3 Giga-byte! Although Dijkstra obtained a reduction of a factor eight by using the symmetry of the structure, the huge matrix couldn't be solved because of the memory restrictions of his computer.

#### 3.3.1.An iteration algorithm

The problem with solving the capacitance is to find the inhomogenous charge distribution. For a perfect conductor the potential is equal in every location in the structure. This fact can be used to find the charge distribution. Imagine a plate that is partitioned with n×n areas with initially an equal charge. It is easy to calculate the electrical force on each element due to all the other elements using Coulomb's law:

$$\mathbf{F}_{1.2} = \frac{\mathbf{q}_1 \mathbf{q}_2}{4\pi\varepsilon_0 \mathbf{R}^2} \cdot \mathbf{a}_{\mathbf{R}}$$
 330

It gives the force on cherge  $q_1$  dependent on a second charge  $q_2$  at a distance R. As a result of the total force due to all other charges charge  $q_1$  will move through the metal in the direction of vector  $\mathbf{a}_R$ . The total force on charge  $q_x$  is:

$$\mathbf{F}_{\mathbf{q}_{\mathbf{x}}} = \frac{1}{4\pi\varepsilon_{0}} \sum_{i=1}^{n^{2}} \frac{\mathbf{q}_{\mathbf{x}} \cdot \mathbf{q}_{i}}{\mathbf{R}_{i}^{2}} \cdot \mathbf{a}_{\mathbf{R}_{i}}$$
 331

Note that the term for x = i must be set to zero because this would give the force of charge  $q_x$  on itself.

If the size and the direction of the force are being calculated for an element, a decision can be made about the direction and step for moving the charge. After this, the next charge area can be evaluated. When all the charge area's are evaluated once and eventually moved, a successive evaluation cycle can be made. After a certain number of evaluations (iterations) all the forces in the plate will be zero.

In pseudo Pascal the method is for one plate:

```
Program Charge_Distribution;
Const N = Size_of_plate;
Var i,j: integer;
A: array[1..N,1..N] of charge;
Begin

(* Initialise *)
For i := 1 to N do
For j := 1 to N do
```

```
While not stop_condition do

(* For every location in the plate..... *)

For i := 1 to N do

For j := 1 to N do

begin

(* .....Calculate the force due to all other charges *)

Get_Force_summation(Force, direction);

If (direction = 'x') and allowed then move_x_direction;

If (direction = 'y') and allowed then move_y_direction;

(* ....And move the charge if allowed *)

end;

(* Evaluate with another program *)

Save_situation;

end.
```

A[i,j] := Init;

The result is the situation where:

$$\mathbf{F} = 0$$

$$\mathbf{E} = \frac{\mathbf{F}}{q} = 0$$

$$\mathbf{V} = \int \mathbf{E} \cdot d\mathbf{l} = \text{Constant}$$

So the potential in the conductor is equal in every location and the charge distribution will be inhomogenous which is the expected situation. From the (constant) potential the capacitance is easy to calculate using the fact that no charge was lost, so  $Q = q_{initial} \cdot n^2$ .

$$C = \frac{Q_{tot}}{V} = \frac{\sum_{i=1}^{n^2} q_i}{V} = \frac{n^2 q_{initial}}{V}$$
332

With the voltage V is the difference between the potentials of both plates using:

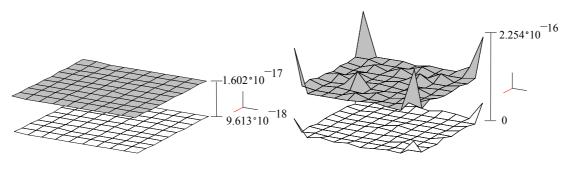
$$V_{\text{plate}} = \frac{1}{4\pi\varepsilon_0} \sum_{i=1}^{n^2} \frac{q_i}{R_i}$$
 333

Using this method, the number of elements is now as big as the number of q's, so for two parallel plates with partition  $n \times n$  a storage of  $2n^2$  numbers is needed, which is 117 kilobyte for n = 100 stored as reals (6 bytes). This gives an improvement of a square root in relation to Dijkstra's method.

#### 3.3.2. Example: finite dual plate capacitor

In Appendix E a listing for a program that calculates the most ideal charge distribution for a dual plate capacitor with partition  $n \times n$ , initial upper-plate charge U and initial lower plate charge L. This is an implementation of the iteration algorithm described in the previous section using Turbo Pascal, it could be described in a "solve block" in MathCad aswell. The very simple iteration method moves just one complete Coulomb at a time (no proportional iteration).

As an example two parallel plates are taken with n = 10 and  $U = 100 (\times 1.602 \cdot 10^{-19} \text{ Coulomb})$  and  $L = 60 (\times 1.602 \cdot 10^{-19} \text{ Coulomb})$ . The gap size is 1. The initial distribution is viewed in figure 3.1a. After 60 iteration steps (evaluations of complete upper and lower plate) the program returns the charge distribution as in figure 3.1b. It is clear that the charge has moved to the edges of the plates as we could expect from the electro magnetical theory [5].



[a] Initial charge distribution

[b] Optimised charge distribution

31 The effect of the iteration algorithm

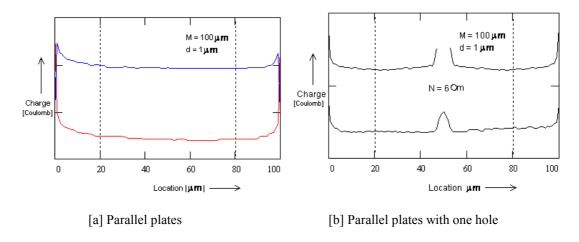
The Pascal program saved the charge distribution to a file. The corresponding potential was calculated with MathCad. With the size units in mm this resulted in:

$$\begin{split} &V_{upper}=49.32mV\\ &V_{lower}=48.78mV\\ &\Delta V=0.54mV, \Delta Q=6.4\cdot 10^{-18}C \Rightarrow C=1.19pF \end{split}$$

The ideal capacitor with size 10×10 mm and gap 1 mm has a capacitance of 0.885pF according to equation 2.2.

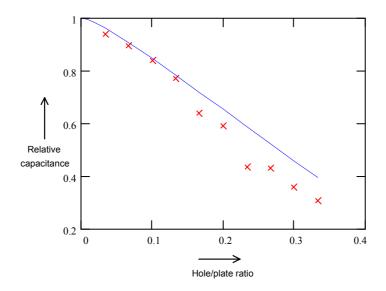
# 3.3.3. Verifying by comparing to the mapping method

To verify the iteration method it was related to the result of the conformal mapping theory. To do this the program listed in Appendix E was adapted to a two dimensional version. Two plates with hundred partitions (each representing one micrometer) were separated by a gap of 1 µm. The initial charge was 20 Coulomb for the upper plate and 10 Coulomb for the lower plate. After 60 iterations the situation had become stable. The program returned the charge distribution of figure 3.12a. Here is M the plate length and d the air gap size. With MathCad the potential of both plates was calculated. To calculate a value for the capacitance the plate was cutted at a size of 60 µm in order to remove the boundary effects. This gave a value for the stored charge. The capacitance that was calculated from this normal capacitor was used as a reference for the one with the hole.



312Charge distribution after a two dimensional iteration

In figure 3.12 a hole with size of 6  $\mu$ m was used, the cutted area was the same as in figure 3.12 so the hole/plate ratio is 6/60 is 10%. With the hole size varying from 20 to 2  $\mu$ m with steps of two micron, figure 3.13was found. The drawn line is calculated with the conformal mapping method.



313Simulation results together with conformal mapping result

It seems that the iterative method fits with the analytical theory. For small holes the difference is smaller than for larger holes (<15%). This can be explained by the accuracy of cutting the capacitor with boundary effects. The calculations should be repeated for much longer plates so that the cutting is less critical.

#### 3.4. Conclusions

By the mathematical method of conformal mapping the capacitance of an infinite plate with an infinite number of holes was evaluated. This method used the periodicity of the structure. Because we are interested in a three dimensional structure this method is not complete. A numerical method was derived to solve three dimensional structures. This numerical method was verified by the analytical method, but not applied to the actual microphone because of time considerations.

In comparison to the old method of Fred Dijkstra an improvement of a square root is obtained in the storage requirement with the simulation method. This is the result of going from a matrix solve-method to an iteration method. The problem with iteration methods is the time consuming calculation and the lower accuracy.

The result of the calculations, obtained with both methods, is that for small holes (actually grooves) the capacitance does not differ a lot from a capacitor without holes. The range of hole sizes where this effect takes place will be larger in the three dimensional case (holes instead of grooves) because the holes are bounded by four edges. So with the microphones the huge loss of capacitance with a hole ratio of 20% as calculated in the previous sections may not be the case.

# 4. Measuring small capacitances

An indication of the state of the microphones can be obtained by measuring its static capacitance. If the value is what we expect, the microphone might work. From the capacitance we can derive the average air-gap thickness or conclude that the microphone is broken or sticked.

# 4.1. The problems of measuring

The capacitance of a microphone (which is in fact a parallel plate capacitor) was given by the very simple formula 2.2 and is repeated here:

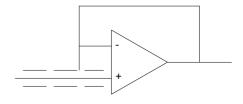
$$C = \frac{\varepsilon_0 A}{x}$$
 4.1

For example, with an air gap x of 3  $\mu$ m and a surface A of 2  $\times$  2 mm the capacitance will be 11.8 pF ( $\epsilon_0 = 8.85 \cdot 10^{-12}$  F/m). This is a very small value and the fluctuations during operation will be even smaller. Therefore a very accurate measurement system is necessary.

A second problem is that the microphones are on a wafer or chip. The only way to contact them is by using a probe station. This will introduce a lot of parasitic capacitances. An easy way to measure the capacitance is by putting it into a passive network and evaluating the response to an applied signal. In the next sections some methods are described to measure the capacitance with an RC-network and an active shielded RC-network is proposed to reduce the parasitic capacitances.

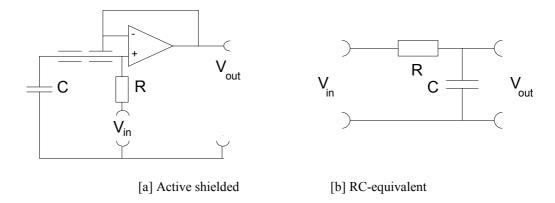
#### 4.2. Active shielded RC-circuits

A parasitic capacitance is only a problem with a non zero voltage between the two conductors. It is possible to reduce the effect of the capacitance to zero by giving the shield the same potential as the wire by adding a unity gain amplifier. This principle is called "active shielding" or "bootstrapping".



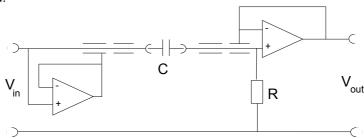
4.1 Bootstrapping

Figure 4.1 can be expanded by adding a signal source and a resistor. Now a RC-network is realised with an active shielded capacitor. Figure 4.2 shows the circuit and the RC equivalent.



42 Active shielding of a capacitor

The problem with this circuit is that one side of the capacitor must be grounded by a rather long wire which still will pick up some noise. So a second unity gain amplifier must be added.



43 Dual bootstrapped capacitor

This is a RC-network with R and C swapped. The value of the capacitance of the microphones is from 1 to 100 pF so if R = 1  $M\Omega$  the -3 dB frequency is between 1.6 and 160 kHz, which is a good range to measure.

With the bootstrapping not only the capacitance of the wires is reduced but also the differential input capacitance of the amplifier. The common input capacitance  $C_{com}$  of the amplifier is not eliminated but becomes parallel to R in the circuit of figure 4.3. The transfer function normally is:

$$H(j\omega) = \frac{j\omega RC}{1 + j\omega RC}$$
 42

and becomes with the presence of C<sub>com</sub>:

$$H(j\omega) = \frac{j\omega RC}{1 + j\omega R(C + C_{com})}$$
43

At the cut off frequency (where  $|H(j\omega)| = -3$  dB and the phase is 45°) an RC product can be measured. The effect of the common input capacitance of the amplifier only is a constant shift in the equivalent C of this product.

A second parasitic capacitance is that of the two probes which are not completely shielded. The bare ends will give a constant capacitance parallel to the unknown capacitance. Once determined for the system this capacitance is no problem because it can be subtracted from the measured value.

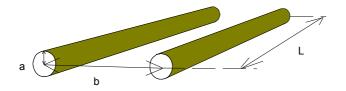
Assume that the probes are ideal parallel wires which have length L and radius a (figure 4.4). Using Gauss's law

$$\iint_{S} \mathbf{E} \cdot \mathbf{e}_{d} ds = \frac{\rho_{v}}{\varepsilon_{0}}$$
 4.4

applying on a concentric cylinder follows:

$$\mathbf{E} = \frac{\rho_{\rm v}}{2\pi\epsilon_{\rm o}rL} \cdot \mathbf{a}_{\rm r} \tag{4.5}$$

With  $\rho_v$  the free charge on the wire and  $\mathbf{a}_r$  the radial vector of the wire.



4.4 Model of two probes to calculate the capacitance

From the electric field the potential can be calculated:

$$V = -\int_{r=a}^{b-a} \mathbf{E} \cdot dl = -\int_{r=a}^{b-a} \frac{\rho_{v}}{2\pi\epsilon_{0} rL} dl \qquad \qquad 4.6$$

Which results in:

$$V = \frac{\rho_{v}}{2\pi\epsilon_{0}L} \ln\left(\frac{b-a}{a}\right)$$
 4.7

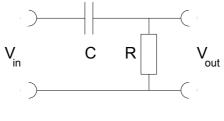
And:

$$C = \frac{Q}{V} = \frac{2\pi\varepsilon_0 L}{\ln\left(\frac{b-a}{a}\right)}$$
 4.8

is the capacitance for two parallel cylindrical wires (probes) with radius a and distance b between their axes. The used Karl Süss probes have a common unshielded area of 7 cm and are between 1.5 and 6 cm from each other (not parallel), the capacitance can be expected to be between 1.8 and 11 pF.

# 4.3. Measurement protocol

This section gives the very basic methods to obtain the value of the capacitor from the transformation that the network does on an applied signal. In figure 4.5 the mentioned RC-network is drawn.



45 RC-Network

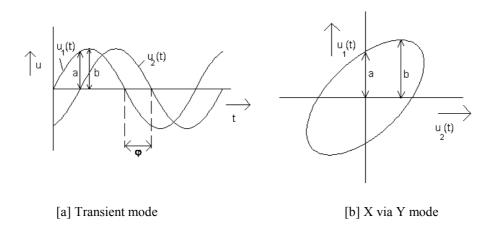
# 4.3.1. Using Lissajous figures

In figure 4.6a two sinus shaped signals are drawn with phase difference  $\varphi$ . The two signals are:

$$u_1(t) = A_1 \cdot \sin(\omega t + \varphi) \tag{4.9}$$

$$\mathbf{u}_2(\mathbf{t}) = \mathbf{A}_2 \cdot \sin(\omega \mathbf{t}) \tag{4.10}$$

With the scope in X via Y mode a Lissajous figure like 4.6b is visible.



4.6 The phase-angle between two signals

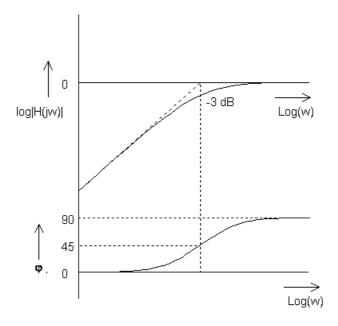
If we examine the points with amplitude a and b we can find:

$$u_1(t_a) = A_1 \cdot \sin(\omega t_a + \varphi) = A_1 \cdot \sin(\varphi) = a$$
  
$$b = A_2$$

This results in:

$$\frac{a}{b} = \sin(\varphi) \tag{4.11}$$

With the bode diagram of an differentiating RC-circuit (figure 4.7) we find that if  $\rho = 45^{\circ}$  we are at the -3 dB frequency at which  $f = (2 \cdot RC)^{-1}$ .



47 Bode plot of differentiatin g RC-circuit

The procedure is:

- Find the frequency at which  $a/b = \sin(45^\circ) = 0.5 \cdot \sqrt{2}$
- Calculate the capacitance by using  $C = (2\pi f_{-3dB} \cdot R)^{-1}$

To find the capacitance it is necessary to manipulate the frequency to find  $f_{-3dB}$ . Fortunately, this can be done very accurately because:

$$\frac{\mathrm{dC}}{\mathrm{df}_{-3\mathrm{dB}}} = \frac{1}{2\pi R f^2}$$
 412

This means that a small error in the adjustment of the right frequency gives an  $1/(2\pi R f^2)$  times smaller error in the calculated capacitance.

This method might be useful to eliminate the common input capacitance. This is because the -3 dB frequency is evaluated, at which this parasitic capacitance only gives a constant shift in the measured capacitance according to the cut off frequency calculated from equation 4.3.

#### 4.3.2. Using the step response

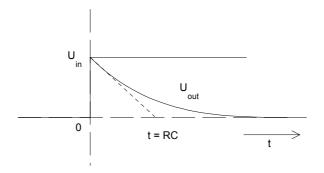
After applying a voltage step of  $V_{in}$  to the circuit of figure 4.5 the response is:

$$U_{out} = U_{in} \cdot e^{-\frac{t}{RC}}$$
 413

The slope at t = 0 is:

$$\frac{dU_{\text{out}}}{dt}\Big|_{t=0} = -\frac{U_{\text{in}}}{RC}$$
 4.14

Graphically the RC-constant can be derived by using figure 4.8. The time where the dashed line cuts the time axis is 1/RC. To get such a picture on the scope we must apply a square voltage with a high enough period (for example 5 times RC).

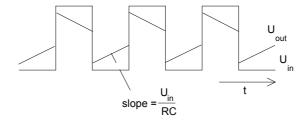


48 Evaluation of the RC -time by using the step response

The accuracy is dependent on how exact one is able to draw the slope line on the used oscilloscope.

#### 4.3.3. Using a square wave

This method is very much like the previous, but now a square wave voltage with a period much smaller than t = RC is used so that a straight lined response is obtained.



49 Evaluation of the RC -time by using a square wave

The slope of the output signal is just like the previous section equal to equation 4.14. The accuracy with both methods is less than with the first (Lissajous) method because an error in the measurement changes the calculated capacitance with the same factor. These two methods also are not guaranteed to give a constant common input capacitance shift as mentioned with equation 4.3 (only the -3 dB frequency has a constant shift, not the complete transfer function).

#### 4.4. Realisation and calibration of the circuit

The circuit of figure 4.3 was realised on an experiment print and placed in an aluminium box. To simplify the realisation an external operation voltage was applied. For better performances the circuit must be realised on a specially designed print with better integrated circuits to reduce the parasitic capacitances.

Table 4.1 summarises some integrated circuits that might be used to make the unity gain follower. If an operational amplifier is used the loop must be externally added, voltage followers have those loop inside.

Table 4.1: Some integrated circuits

Туре	Function	Cinput [pF]	BW [MHz]	Ibias
μΑ 741	OpAmp	1.4	1	30 nA
CA 3140	OpAmp	4.0	4.5	1 pA
LF 356	OpAmp	3	5	8 pA
TDB 041	OpAmp	?	0.5	3 pA
LH 0033	V-follower	8	200	10 nA
LM 310*)	V-follower	1.5	20	2 nA

<sup>\*)</sup> Requires a 10 kWresistor at the input

The LF 356 operational amplifier was chosen because this one combines a low input current (due to a FET-input circuit) with a large bandwidth, without having a too large input capacitance. The price is very low in contradiction with the video amplifier LH0033 which costs fl200,-.

The first test was with a capacitor just at the probe-plugs on the box. With the Lissajous figure method we might expect that the measured capacitance is just the applied capacitance plus the common capacitance of the output amplifier. The results are in table 4.2

Table 4.2: Measured values with the circuit of figure 4.3

Capplied [pF]	Cmeasured [pF] (Without probes)	Cmeasured [pF] (With probes)	Cinput [pF]	Cprobes [pF]
none	-	10.2	?	?
1	7.8	12.0	6.8	4.2
10	16.9	22.1	6.9	5.2
20	26.8	30.6	6.8	5.4

We can conclude that the input capacitance of the used voltage follower is about 6.8 pF (two times the input capacitance from the documentation) because a constant offset is found. The parasitic capacitance due to the unshielded tips of the probes can be calculated from the measurements with probes by subtracting the opamp input capacitance and the actual value. The value of about 5 pF fits with the calculated capacitance.

The capacitance of the probes fluctuates with the relative humidity of air and their poition. To eliminate all types of parasitic capacitances two frequencies must be measured using the Lissajous method: the unloaded and the loaded cut-off frequency:

$$C = \frac{1}{2\pi R f_{loaded}} - \frac{1}{2\pi R f_{unloaded}} = \frac{1}{2\pi R} \left( \frac{1}{f_{loaded}} - \frac{1}{f_{unloaded}} \right) 4.15$$

As a test some capacitive structures of size  $2.5\times2.5$  mm and air gap 3  $\mu$ m were measured. All capacitors were around 35 pF and the theoretical capacitance (using equation 2) is 18 pF. We can conclude that the air gap was somewhat thinner than 3  $\mu$ m.

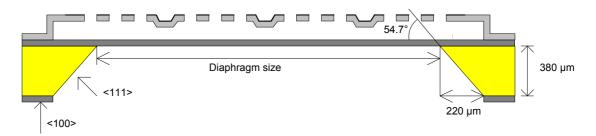
# 5. The microphone design

As the starting point of the design of the new microphone, the design of Patrick Scheeper was used. To be able to compare the new microphone properties to the old one the design parameters were taken identical. In this chapter the development of the new masks is described.

#### 5.1. The functions of the masks

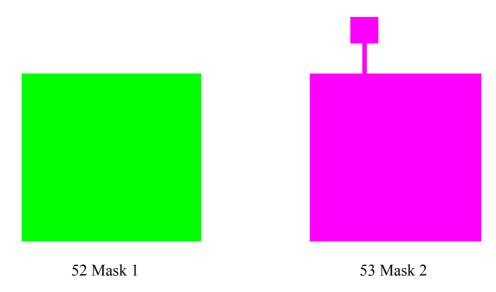
Mask 1 has two functions: it defines the silicon etch area on the backside and it is used to shape the sacrificial layer on the front side. Because it is used on both sides a contact copy will be necessary to keep the black side of the mask in contact with the wafer (to avoid problems with the exposure).

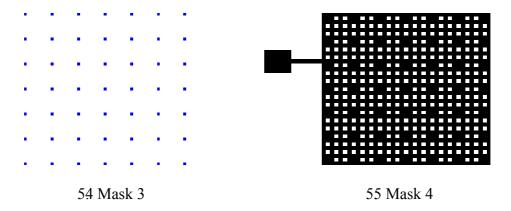
The membrane size is defined by the size of the silicon etch area mask. Figure 5.1 shows that with a 380  $\mu$ m thick wafer the silicon etch area should be two times 220  $\mu$ m bigger than the desired membrane size because of the angle in the silicon due to anisotropical etching of <100> silicon. The size of the square is 1.940 mm (desired diaphragm size + 2 × 220 $\mu$  m).



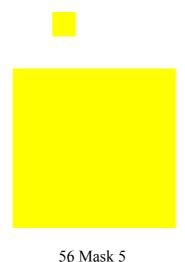
51 The effect of the angle in the silicon on the mask design

Mask 2 defines the size of the diaphragm conductor. Actually this is the new mask that will allow us to make the diaphragm contact on the front. The size is  $10~\mu m$  smaller on each side then mask 1. The connection pad is  $320\times320~\mu m$ .





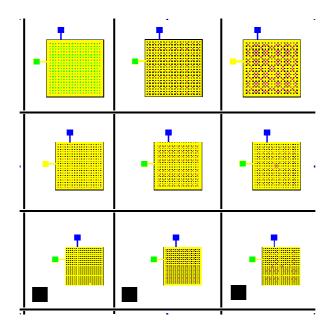
Mask 3 is used for a short etch of the aluminium to obtain the diaphragm supports. The size of mask 4 which defines the backplate conductor and act as a window for the acoustic hole etching is equal to that of mask 2. The connection pad for this layer is located on another side of the microphone than the diaphragm pad.



Finally mask 5 defines an area in which the etch of the silicon nitride can take place. Also the this mask will expose the diaphragm pad.

## 5.2. The mask units

Because the memory size of the mask design program CLE was not sufficient to hold the complete masks with the huge amount of acoustic holes (probably more that 10.000 objects), smaller units of nine microphones each were designed.



57 One mask unit with nine microphones

Figure 5.7 shows one unit. In table 5.1 the sizes of the membranes and hole/conductor ratios (A) of the microphones are given. The size of one unit is  $15 \times 15$  mm. The lines between the microphones are in the (backside) silicon etch mask, they make the separation of the devices easier. The alignment points are in each unit and will be discussed in section 5.3.

Table 5.1: Sizes of the microphones

Table 5.1. Sizes of the interophones						
Type 1a membrane: conductor: hole size: #holes: #supports: A:	2.5×2.5 mm 2.88×2.88 mm 70×70 μm 312 49 18.4%	Type 1b membrane: conductor: hole size: #holes: #supports: A:	2.5×2.5 mm 2.88×2.88 mm 70×70 µm 400 100 23.6%	Type 1c membrane: conductor: hole size: #holes: #supports: A:	2.5×2.5 mm 2.88×2.88 mm 80′80 μm 289 136 22.3%	
Type 2a membrane: conductor: hole size: #holes: #supports: A:	2.0×2.0 mm 2.41×2.41 mm 60×60 μm 312 49 19.3%	Type 2b membrane: conductor: hole size: #holes: #supports: A:	2.0×2.0 mm 2.41×2.41 mm 60×60 µm 324 81 20.1%	Type 2c membrane: conductor: hole size: #holes: #supports: A:	2.0×2.0 mm 2.41×2.41 mm 60×60 μm 361 68 22.4%	
Type 3a membrane: conductor: hole size: #holes: #supports: A:	1.5×1.5 mm 1.93×1.93 mm 50×50 μm 312 49 20.9%	Type 3b membrane: conductor: hole size: #holes: #supports: A:	1.5×1.5 mm 1.93×1.93 mm 50×50 µm 324 81 21.7%	Type 3c membrane: conductor: hole size: #holes: #supports: A:	1.5×1.5 mm 1.93×1.93 mm 50×50 μm 361 80 24.2%	

The conductor size (which is the same for both the membrane and the backplate conductor) exceeds the membrane. The hole/conductor ratio can be calculated as follows:

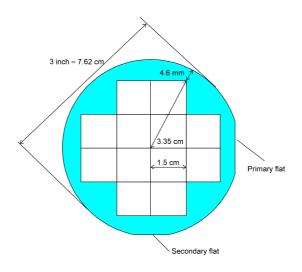
$$A = \frac{\# \text{holes} \cdot \text{holesize}}{\text{conductorsize}}$$
 51

From experience this ratio was set to about 20% by fitting the hole ratio and size to the conductor size. The number of supports was assumed to be unimportant. During placing the holes and supports, the symmetry of the device was kept in mind.

In the same squares of structures 3a t/m 3c some test structures are defined. These are all "microphones" with a diaphragm of  $0.3 \times 0.3$  mm but without a backplate. From this structures an indication is given if the sacrificial layer etch does not modify the diaphragm conductor.

#### 5.3. Structure of the complete wafer

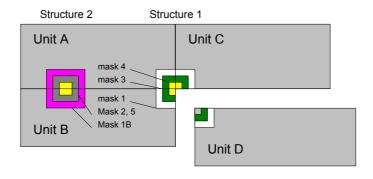
The unit drawn in figure 5.7 can be repeated 12 times on one 3 inch wafer. The structure has a distance of 4.6 mm to the edge of the wafer.



58 Placement of the units on the wafer

The primary flat of the wafer must be parallel to the microphones else the anisotropic etch of the silicon will give problems.

The alignment points of the masks are defined in each unit. The edges of four units form concentric squares together (structure 2) and the sides of two units form another set of squares (structure 1).



59 The alignment points

The procedure is:

- Mask 1B on the backside.
- Align mask 2 on the frontside on mask 1 with the double side aligner using structure 2.
- Align mask 1 on mask 2 using structure 1.
- Align mask 3 on structure 1.
- Align mask 4 on structure 2.
- Align mask 5 on structure 2 (mask 5 has a hole instead of a dot as alignment point).

Table 5.2 gives a summary of the used masks.

Table 5.2: Summary of the masks

Mask	Function	Polarity	Resist
1B	Silicon etch area (contact copy of mask 1)	+	-
1	Sacrificial layer shape	+	+
2	Diaphragm conductor	+	+
3	Diaphragm supports	+	-
4	Backplate conductor with acoustic holes	+	+
5	Sacrificial layer etch window	-	+

Appendix B contains plots of the masks 1 to 5 directly plotted from the mask design program CLE.

# 6. The silicon microphone process

The silicon process was completed two times during the project. The first batch had a lot of problems that were merely solved during the second run. After a description of the problems during the processing, the measured results with the microphones are given.

## 6.1. Problems occurring during first run

The first processing was done with three 3 inch wafers. The conductors were made of 30 nm gold with 30 nm titanium as adhesion layer.

During exposure of a wafer in contact with a mask this mask sometimes keeps stuck to the wafer (especially with thicker photo-resist or sticky negative resist). A method to separate them is putting the mask for thirty minutes in acetone and then pushing the wafer off. To avoid sticking a Teflon later might help. The Teflon is applied by spinning (liquid FC722 manufactured by 3M) at a speed of 1000 rpm on the mask followed by a drying step of 120°C for some seconds. The Teflon can be removed by putting a strong water jet on the mask.

Only one wafer came through the KOH anisotropic etch of the substrate. Although this is a well known process it requires a certain skill to avoid breaking down of the very thin (some microns) microphone membranes. In the next section this step is therefore evaluated.

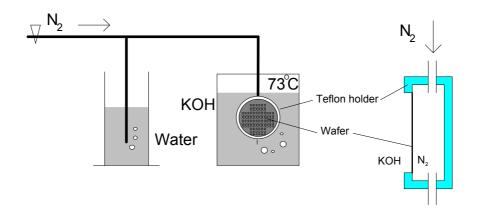
The actual aim of the processing was to see what happens to the new gold layer on the membrane. With the masks discussed in the previous chapter the gold on the backplate acts as a mask during reactive ion etching of nitride and some gold on the membrane acts as an etch stop. During this step the gold disappeared at both locations. Patrick Scheeper did not have this problem because he used resist as a mask and had not the gold as etch stop. It is possible to put resist on the backplate in the new design although the alignment becomes very critical and the problem with the etch stop function is still not removed.

The cause of the problem and some solutions are discussed in the next section.

Another problem was the freeze drying after the sacrificial layer etch. This is to avoid large capillary forces during drying of micromechanical structures, but the freeze drying itself is a very tricky skill so a section is devoted to this.

### 6.1.1. Anisotropic etching of silicon with KOH

In an early stage of the silicon process it is not convenient to etch through the complete wafer because of the risk of damaging the devices. The last  $80~\mu m$  should be etched just before the final sacrificial layer etching. To protect the front side of the wafer with the structures (the KOH-etching is from the backside) the wafer is placed in a Teflon holder which cover the frontside. This is why only complete wafers can be etched so the process is not allowed to fail.



61 KOH etching in a Teflon holder

The  $N_2$  gas garantees a higher pressure in the holder to avoid leakage. If this pressure is too large the thin microphones (containing a membrane, a sacrificial layer and the backplate) will be blown out. To avoid this the beaker with water is a pressure buffer. In the MESA lab the place were the KOH-etching is done is at the end of the  $N_2$  supply so huge fluctuations in the flow can be expected.

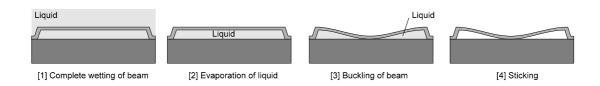
One wafer was damaged because of a too low pressure (KOH liquid came into the Teflon holder) the other one because of a too high pressure (one microphone broke out). Because the etching requires some hours it is not possible to watch the pressure constantly.

In future attention should be paid to a valve that garantees a constant pressure. Until then it is better to rely on a completely closed holder without using the  $N_2$  flow.

Another problem during the etching is that a small pinhole in the membrane nitride is followed by a fast etching of the aluminium and results in a leak in the wafer.

#### 6.1.2. Freeze drying

During drying of small structures the capillary forces can cause the structure to collapse (figure 6.2 picture 1-3). If the region of contact between beam and substrate is big enough and the tension in the beam too small the beam will remain stuck to the substrate (figure 6.2 picture 4). This complete process is called sticking and is one of the most important yield-lowering phenomena of surface micro machining [9].



62 The process of buckling and sticking

There are three options to lower the sticking possibility:

• To lower the problem of sticking the backplate was supplied with diaphragm supports. These are 0.5 µm high dips in the backplate, created by a local etch of the sacrificial layer. The aim is to decrease the contact area during phase [3] of figure 6.2 in order to lower the risk of sticking. Those supports have a surface of

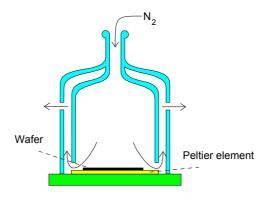
- ther own however and leave the possibility of sticking at these tips. Another option is that the membrane keeps stuck between two supports.
- Another option which is well known at the department of micromechanics of the University of Twente is to apply a dry sacrificial layer etch technique, for example with the reactive ion etch method. This requires a different sacrificial layer material from aluminium so this method can not applied here.
- It is possible to avoid phase [3] by freezing the liquid in phase [1] and let the ice sublimate. There will be no capillary forces now. This process is called freeze drying.

For the freeze drying Patrick Scheeper used a different method from what has become the standard method in the MESA lab now. His method was [2]:

- After completion of the sacrificial layer etching an etch stop of deionised water was applied for at least 10 minutes.
- As sublimating material water would last to long so a mixture of methanol and water (2:1) was used. Rinse for 30 minutes.
- The wafer was placed immediately free hanging in a vacuum chamber. The pressure in the chamber was lowered to 0.4 mbar so that the water-methanol mixture immediately froze to a soft ice.
- The sublimating lasted about 60 minutes. To avoid condensation of water after opening the chamber was heated for 15 minutes.

Now the freeze drying has become more applied, a permanent setup with a slightly different protocol is installed in the cleanroom:

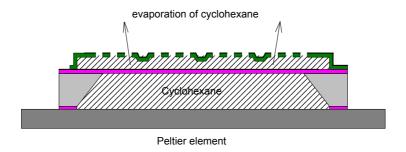
- After sacrificial layer etch in water as etch stop.
- Place the wafer with additional water in isopropanol (IPA) for one hour to remove the water. Because it has a freeze point of 4°C and it sublimates quite fast, cyclohexane will be the freeze dry liquid. The rinsing with IPA is necessary because cyclohexane is hydrophobic and the water would not get away.
- Move the wafer to a beaker with cyclohexane for 30 minutes.
- To verify whether all water is out of the structure there is a method to check the cyclohexane. Cyclohexane with IPA gives a clear solution, cyclohexane with a little bit of water gives a messy mixture if IPA is applied. So by putting some IPA in the beaker the presence of water can be detected. Water gives troubles during freeze drying because it sublimates very slowly and it has large variations in vhume around the freeze point.
- The freeze dry bottle is drawn in figure 6.3. The wafer is put in contact with a peltier element to make the temperature about -10 °C. A nitrogen gas flow is added to remove evaporated cyclohexane which fastens the sublimation and avoids water to condense on the cold wafer.



63 The freeze dry bottle

• After about half an hour it is visible that the ice has disappeared. The peltier element is set to heating (about 25 °C) without opening the bottle. This is also to avoid condensation of water.

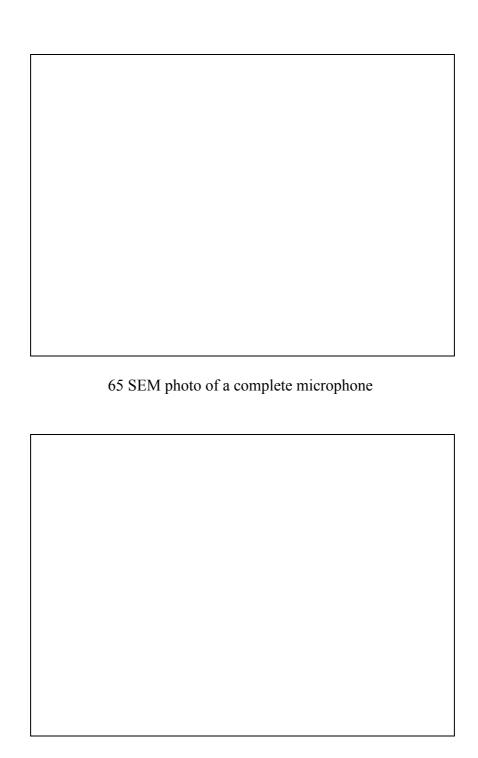
The problem with this new method is that it was meant for surface micromechanical structures. The microphones have a hole on the backside (because of the isotropic etch of silicon) so cyclohexane that freezes in this hole will never be able to sublimate for it is in contact with the peltier element. The old method did not have this problem because the wafer was free hanging.



64 Problem during freeze drying

Because the freeze drying lasted too long the process was stopped by heating the system before all the ice was sublimated (closing time in the MESA lab). Some microphones were completely pulled in because of the capillary forces in the cave under the microphone. Others had only pull-in effects between the backplate and the membrane. The last remained stuck mostly, the first were completely broken.

Picture 6.5 shows a SEM (Scanning Electron Microscope) photo of a microphone. The characteristic view is the backplate with the acoustic holes. The bright area somewhat to the right of the middle indicates a distance between the membrane and the backplate. In the other area sticking occurred. This area looks like a not focused region but it isn't: the SEM measures an difference in reflection intensity here which gives another brightness.



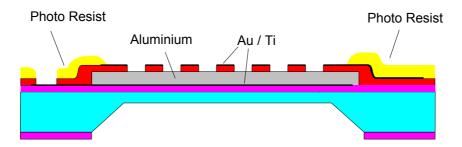
66 Close up

To avoid the problem of storage of liquid under the wafer it must be placed on a certain distance from the surface of the peltier element. Probably the temperature will still be lower than the freeze point of cyclohexane.

## 6.1.3. Reactive ion etching of nitride with gold as a mask

The gold on the backplate has a special function during processing. In the conventional microphone process the resist that was applied to etch the holes in backplate conductor, was used to etch the silicon nitride aswell. With the new method

this is no longer possible because the nitride must have a hole now to clear the membrane conductor pad (see the difference in mask 4 and 5 in section 5.1). Partially the gold conductor on the backplate was used as a mask during RIE etching of nitride. This made the alignment of mask 5 a lot less critical. The etch stop was the aluminium in the air gap and the membrane gold at the membrane pad. Figure 6.7 gives the situation just after the RIE etching is completed.



67 The situation just after the RIE etching

The problem was that the gold at both areas that are not covered with resist disappeared during the etching. This can be seen in the SEM picture of figure 6.5 were a bright ring of gold has remained at the edge of the backplate that was covered by resist during etching. I assumed that this happened by physical sputtering. The plasma in the RIE machine has a very high intensity and the bombardment with ions results in emission of the gold. This is plausible because gold has a very high sputter rate. If this is the cause there are some possibilities to solve the problem:

- Choose another conductor with a lower sputter rate Alternatives are for example chrome and titanium which are less easy to apply. The problem with chrome is that it has a large tensile stress so only very thin layers are allowed.
- An indication of the bombardment intensity is given by registering the bias voltage. In the next table some compositions for nitride etching are given:

Table 6.1: Parameters for RIE etching of silicon nitride

	I: Normal	II: Low V <sub>bias</sub>	III: High pressure	IV: Low energy
Temperature	25°C	25°C	25°C	25°C
Pressure	10 mTorr	75 mTorr	30 mTorr	20 mTorr
Energy	75 Watt	75 Watt	75 Watt	40 Watt
CHF <sub>3</sub>	25 seem	=	25 sccm	=
SF <sub>6</sub>	-	54 sccm	-	5 sccm
$N_2$	-	-	-	50 sccm
$O_2$	5 sccm	-	5 sccm	-
Rate	77 nm/min	150 nm/min	44 nm/min	67 nm/min
V <sub>bias</sub>	583 Volt	8.6 Volt	unknown	368 Volt

The bias voltage is not only dependent on the used gasses but also on the size of the wafer, the etch area, the target material and many more parameters. The values in the table are measured once with quarter wafers and give an indication of the magnitude with each mentioned set of parameters. It will be clear that method II gives a lower bias voltage and so the sputtering effect will be lower (Henry Jansen, TDM MicMec).

- Sputtering becomes less probable if the pressure is higher. Method III gives a set of parameters with higher pressure (Dion Oudejans, BIO-sensors).
- Avoid a lasting exposure to the bombardment by putting resist on the gold. This might be a critical alignment procedure and doesn't prevent etching of the etch stop. So stop at the right time and combine this option with an adaptation of the gas mixture.

Due to the loss of two wafers during KOH etching and the third during the RIE etch it was not possible to measure anything. With learning of the problems of the first processing, the process was adapted.

### 6.2. Improved process

The second processing was done with two wafers. The following adaptations were made:

- Because the aim is the realisation of an inner conductor layer the problem of the KOH etch technique was omitted by not doing it. This saves some time and it is of no importance because the "microphones" can be characterised by measuring the static capacitance and by optical inspection. Another advantage is that the problem with freeze drying is now gone and the standard method can be applied.
- Two adaptations mentioned in the previous section for sustaining the RIE etch were applied. On one wafer the gold conductors were exchanged by chrome because this metal has a lower sputter rate. Etch method IV was applied. The disadvantages of chrome are the tensile stress and the fast oxidating (higher resistance and worse contacts). A second wafer was initially the same as the ones in the first run (gold) but was etched with nitride etch method II (using a quartz target).

#### 6.3. Results

Both wafers finished the processing. Some remarks are listed here:

- The chrome was much too thick on both the membrane and the backplate because of an improper crystal which acts as an imprecise thickness monitor during evaporation. A thickness of 200 nm was measured with the Dektak surface profiler.
- This thick chrome layer resulted in an extremely high tensile stress: if a backplate was scratched with a needle it broke and curled.
- Just after finishing the process the chrome was easy to contact. After a few days a series contact resistance of about  $500\Omega$  was measured. This is probably due to oxidation of the chrome
- The gold wafer had bad step coverages which is a problem with the pads. The wire from the backplate pad to the backplate conductor was broken with about 70% of

the microphones. The chrome did not have this problem probably because it was much too thick.

• Due to the same problem the coverage of the gold on what will be the backplate supports was bad. This resulted in etching of the supports (figure 6.8).



68 Problem because of bad coverage of the gold

• With some capacitors the capacitance was measured. The result is given in table 62 and came from two quarters of wafers, one with gold and one with chrome.

Table 6.2: Measured capacitances

	Measurements				Calculated	
Size	Ccr	<b>d</b> Cr	CAu	dAu	Ccalc	Cstick
$[mm^2]$	[pF]	[µm]	[pF]	[µm]	[pF]	[pF]
1.5×1.5	$22 \pm 20$	≈ 0.7	6	≈ 3.1	6.1	83.6
2.0×2.0	$59 \pm 20$	≈ 0.4	-	-	10.9	148.7
2.5×2.5	$54 \pm 20$	≈ 0.8	$24 \pm 6$	≈ 2.1	17.1	232.3

The last two columns are repeated from table 3.1. the third and fifth columns are the calculated thicknesses of the air gaps from respectively columns 2 and 4. It can be concluded that the chrome wafer had some sticking problems. The gold wafer looks quite well.

• A method to look under the backplate is putting a piece of tape on the capacitor and ripping it off. The chrome types showed a perfect clean membrane. The gold types however showed a messy nitride. This can partially be explained by the rests of the broken supports but it was also clear that under the backplate holes the gold was etched. An explanation is that the gold has alloyed with the aluminium due to a high temperature step (PECVD?) and became fragile for aluminium etching.

#### 7. Conclusions and recommendations

This chapter contains a summary of all results and conclusions. Some conclusions are new because they combine different sections. Also a number of recommendations is given.

- Some "microphones" without etched substrate were successfully processed in the MESA laboratory using a new design. In the new design both conductors (backplate and diaphragm) can be accessed on the frontside.
- In the conventional silicon microphone process the conductors were made of gold. This gave some problems:
  - 1. The gold on the diaphragm seemed to alloy in contact with the aluminium. The cause can be the temperature of about 300°C used for the silicon nitride etching. The gold is being damaged, especially under the acoustic holes during the sacrificial layer etching with a H<sub>3</sub>PO<sub>4</sub>/CH<sub>3</sub>COOH/HNO<sub>3</sub> solution.
  - 2. Gold has a bad step coverage which results in a bad connection between a pad to put a probe on and the backplate conductor. Another consequence is that some bad covered diaphragm supports are damaged because the under lying nitride are being etched with RIE.
  - 3. The gold was very weak and was easily removed by scratching with a probe.
  - 4. During RIE etching of the acoustic holes the gold disappeared. Not only on locations where it acted as a mask (which can be avoided), but also if it was used as etch stop. Probably the gold was physically sputtered which can be expected because of it's high sputter rate.
- The sputtering effect of gold in the RIE machine can be minimised by using a special etch method. This method combines an increased pressure with a decreased bias voltage. Some good results were obtained.
- Better results were obtained by using a complete different metal. With chrome layers the advantages were:
  - 1. A clean membrane conductor in the microphone showing the same colour as the backplate conductor.
  - 2. Better coverage of steps. The layers were somewhat too thick however.
  - 3. Chrome can be used as a mask during RIE etching of silicon nitride. It endures the normal etching mixture.

#### Some problems were:

- 1. Fast oxidation after processing. This resulted in a bad contact with the probes and an enlarged series resistance which lowered the accuracy of the measurements.
- 2. It is more difficult to apply a layer.
- 3. Chrome has a large tensile stress so only very thin layers can be applied.
- The capacitance of a microphone with a perforated backplate is hard to calculate from Laplace's law. Two other options were evaluated:
  - 1. First the capacitor was imaginary split into an infinite equal units of finite capacitors with one hole each. For such a unit an equivalent ideal capacitor

was calculated using the conformal mapping method. With this the capacitance of the mapped capacitor was mapped to the desired one.

The problem with this method is that it is a two dimensional version because we are restricted to the complex area. In the three dimensional equivalent, the holes in the mapping method are infinite grooves.

2. The second method can be used for three dimensional structures, it is an iterative method. The iteration algorithm converts to the ideal charge distribution. From the charge distribution the potential at every point in the area can be calculated and so the capacitance.

This method is the successor of a method developed by Fred Dijkstra [8] who tried to solve the charge distribution by evaluating matrices. His method was not a success because it would take too much computer memory to solve a microphone. The new iterative method exchanges the memory requirements (improvement of a square root of the partition size) by time consumption.

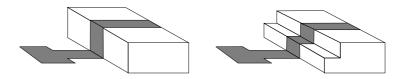
Although the iteration algorithm was not applied to the actual microphone, a verification was made by comparing a two dimensional version of the algorithm to the mapping method. Both methods had the same result.

- The models showed that for small holes (a hole ratio of some percents, depending on the gap size) the presence of the holes does not change the capacity. For larger holes the decrease in capacity is larger than is the case with an ideal capacitor with parallel fieldlines.
- In practice the capacitance of the microphones could be predicted by using the ideal finite capacitor model as if there were no holes. Probably the effect with small holes described with the previous point, is much important in the three dimensional case. Because a hole is being bounded by four edges, the fringing effects will eliminate the effect of the hole. This was concluded with microphones with hole ratio's of about 20%
- A measurement system was developed to measure small capacitances (1 pF to 1 nF) of structures on a wafer. The structure was placed as part of an active shielded RC-circuit.
- The most important paracitic capacitances during measuring are the unshielded probes and the common input capacitance of the used OpAmps. These are parallel to the unknown structure and can easily be eliminated by chosing the right method for measuring.

#### Recommendations:

- Because chrome has some disadvantages, in future other metals can be evaluated or the process must be optimised.
- The wire going from the backplate pad to the actual backplate was broken many times due to the bad step coverage of the conductor material. Prevent the problems with the bad coverage of the backplate pad by using a more gradual step. During

etching of the diaphragm supports in the sacrificial layer a two step pad connection is easy realised without increasing the number of masks.



71 Single step and multi step

- For future research it can be interesting to optimise the iteration algorithm and apply it on a three dimensional structure. If a normalised graph is made once all microphone designers can use this. To improve the algorithm a faster conversion can be obtained by using weighted iteration steps.
- For a higher yield the microphones were simplified. In future a realisation and measurement with complete microphones can finish this project. The microphone can then be dynamically qualified.

# Appendix A: The silicon microphone process

Here is a description of the process steps that gave the best results and can be recommended for further research.

#### Wafers

• Size: 3 inch;

• Thickness: 385- 415μ m (measured 400 μm);

• Flatness:  $\leq 3 \mu$  m;

Material: cz-grown, p-type silicon;
Crystal direction: <100>, alignment ± 1;

#### Standard wafer cleaning

- Fuming 100% HNO<sub>3</sub> dip,  $\geq$  5 minutes to remove organic pollution;
- Second fuming 100 % HNO<sub>3</sub> dip,  $\geq$  5 minutes;
- Quick dump rinsing until conductivity  $< 0.1 \mu S$ ;
- Hot HNO<sub>3</sub> dip,  $\geq$  15 minutes to remove metallic contaminants;
- Quick dump rinsing until conductivity  $< 0.1 \mu S$ ;
- Dry spinning

### LPCVD Si<sub>x</sub>N<sub>v</sub> deposition

Parameters:

 $\begin{array}{cccc} Temperature: & 850^{\circ}C; \\ Pressure: & 200 \text{ mTorr}; \\ SiH_2Cl_2: & 70 \text{ sccm}; \\ NH_3: & 18 \text{ sccm}; \\ Time: & 40 \text{ min}; \\ Expected thickness: & 0.24 \mu \text{ m}; \\ Color: & green; \end{array}$ 



#### First mask (on backside)

Standard lithography procedure:

- Spinning HMDS on backside;
- Negative photoresist (ICT3) on backside;
- Prebake 20 minutes at 90°C;
- Diaphragm mask GL-1B on backside, alignment // primary flat;
- Exposure and development in xylene;
- Rinsing with IPA and spin dry;
- Hardbake 30 minutes at 130°C (not actually necessary for RIE etch);

Reactive ion etching (RIE) of Si<sub>x</sub>N<sub>v</sub>:

Parameters:

Temperature: 25C; Pressure: 10 mTorr; Power: 75 W; CHF<sub>3</sub>: 25 sccm; O<sub>2</sub>: 5 sccm;

Time:  $\pm 3 \text{ min (because etch rate is } 13 \,\mu\text{m/min)};$ 

Strip resist with fuming 100 % HNO<sub>3</sub>



## Incomplete silicon etch

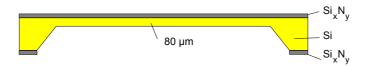
Etchant: 33 wt. % KOH at 73°C

(for example 1500 ml  $H_2O$  with 750 g  $HNO_3$ );

Etch time: 300 minutes, because etch rate theoretically 40 μm/hour;

Intended depth: 300µ m (about 3/4 of the wafer thickness);

In fact the temperature was  $68^{\circ}$ C so the etch rate was smaller, I measured an etch-depth of 245  $\mu$ m with the microscope;



#### **Definition of the diaphragm conductor**

Cr evaporation on front: 50nm;

Standard lithography procedure (positive resist S1818, mask GL-2, developer 351);

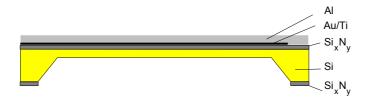
Etching with Cr etchant about 30 seconds (optical stop);

Remove resist with fuming HNO<sub>3</sub>;



#### **Definition sacrificial layer**

Evaporation of aluminium on frontside: thickness: 3  $\mu$ m; Used device is the Varian E-beam;



#### **Definition sacrificial layer**

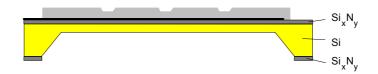
Standard lithography procedure (positive resist S1818, mask GL-1); Al etch: etchant is phosphoric acid, etch until green nitride;



#### **Etching diaphragm supports**

Standard lithography procedure (negative resist, mask GL-3);

Al etch: etchant is phosphoric acid, etch 0.5 µm (etch rate is 35 nm/min);



## P enhanced chemical vapour deposition (P

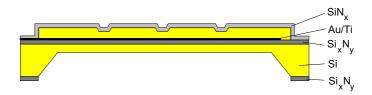
x on front side

Process parameters:

Temperature: 300C; Pressure: 650 mTorr; Power: 20 W; Frequency: 13.56 MHz; SiH<sub>4</sub>/N<sub>2</sub> (2%): 2000 sccm; NH<sub>3</sub>: 10 sccm;

The NH<sub>3</sub> flow exceeds 7 sccm so a tensile layer is deposited (according to Patrick Scheeper [2]).

Thickness: 1 µm



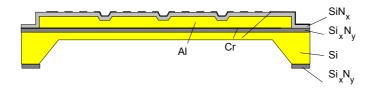
#### Definition of backplate electrode

Cr evaporation on front: 50 nm;

Standard lithography procedure (positive resist);

Etching with Cr etchant;

Remove resist with fuming HNO<sub>3</sub>;

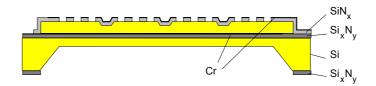


## RIE etch of SiN<sub>x</sub> acoustic holes

Process parameters:

Temperature: 25C; Pressure: 20 mTorr; Power: 40 W; SF<sub>6</sub>: 5 sccm; N<sub>2</sub>: 50 sccm; Time: 15 min;

Strip resist with fuming 100 % HNO<sub>3</sub>



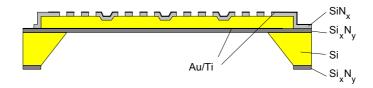
#### Silicon etch

Etchant 33 wt.% KOH at 73°C;

Etch time 90 minutes;

Place wafer in holder;

Intended depth: until nitride, green color;



## Sacrificial layer etching

Solution:  $H_3PO_4$  80;

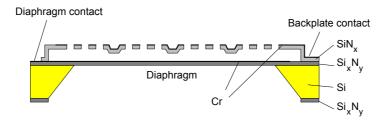
CH<sub>3</sub>COOH 5; HNO<sub>3</sub> 5;

H<sub>2</sub>0 10;

Temperature:  $50\overline{C}$ ;

Etch time: 3.5 hours;

## Freeze dry



# Appendix B: The masks

# Appendix C: Viewing a transformation with MathCad

When a conformal mapping transformation formula is derived it can be viewed very easy by using the mathematical calculation program MathCad. The next listing is a complete MathCad 4.0 for Windows file drawing the result of the calculation of the field at the edges of a finite dual plate capacitor (equation 3.1). This was derived in section 3.2.1.

Air gap: a := 1

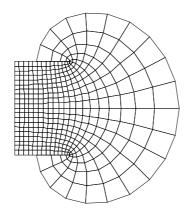
Potential: V0 := 1

Transformation:  $z(w) := \frac{a}{\pi} \cdot (e^w + w + 1)$ 

Potential infinite capacitor:  $V(w) := V0 \frac{Im(w)}{\pi}$ 

Scaling of parameters and filling of parametric plot:

$$\begin{split} u &:= 0..20 \qquad v := 0..20 \qquad & w(u,v) := \frac{u-15}{10} \cdot \pi + i \cdot \frac{v-10}{10} \cdot \pi \\ Mx_{u,v} &:= Re(z(w(u,v))) \qquad My_{u,v} := Im(z(w(u,v))) \qquad Mz_{u,v} := V(w(u,v)) \end{split}$$



Mx, My, Mz

This parametric plot is obtained by making a 3D plot (press Ctrl + @) and giving the three matrices as axis. Set "Tilt" to  $90^{\circ}$  and rotation to  $0^{\circ}$ .

# Appendix D: Solving the equivalent capacitor using **MathCad**

This MathCad 4.0 listing solves the length L for the equivalent dual plate capacitor for a given perforated configuration with holesize N, length M and plate distance d.

Transformation formula:

$$z(w,a,b,K) := -K \cdot \left( a \cdot \coth\left(\frac{w}{2}\right) + \frac{b^2 - a^2}{2 \cdot a^2} \cdot w \right)$$

Gap thickness:

$$d(a,b,L,K) := \left| -\frac{b^2 - a^2}{2 \cdot a^2} \cdot K \cdot \pi \right|$$

Plate size: 
$$M(a,b,L,K) := -2 \cdot K \cdot \left( a \cdot \frac{e^{0.5 \cdot L} - 1}{e^{0.5 \cdot L} + 1} + \frac{b^2 - a^2}{4 \cdot a^2} \cdot L \right)$$

Hole size:

$$u_{N}(a,b) := \ln \left[ \frac{2 \cdot a^{3} + b^{2} - a^{2} + 2 \cdot \sqrt{\left[\left(a^{3} + b^{2}\right) - a^{2}\right] \cdot a^{3}}}{b^{2} - a^{2}} \right]$$

$$N(a,b,K) := z\left(u_N(a,b),a,b,K\right)$$

Parameters of the perforated plate (units µm):

$$d_{given} := 3$$
  $M_{given} := 100$   $N_{given} := 50$   $L_{d} := M_{given}$ 

Initial values:

$$a := 1$$
  $b := 2$   $K := -1$   $L := M$  given

Solve block:

**GIVEN** 

$$d_{given} = d(a,b,L,K)$$
  $b > a$ 

$$M_{given} = M(a, b, L, K)$$
 L>2

$$N_{given} = N(a,b,K)$$

$$\begin{bmatrix} a \\ b \\ K \\ L \end{bmatrix} := Minerr(a, b, K, L) \qquad \text{Result:} \qquad \begin{bmatrix} a \\ b \\ K \\ L \end{bmatrix} = \begin{bmatrix} 3.406 \\ 3.646 \\ -13.123 \\ 11.651 \end{bmatrix}$$

$$C_{eq} := \frac{L_{d} \cdot L}{\pi} \cdot 8.85 \cdot 10^{-12} \qquad C_{ref} := \frac{L_{d}^{2}}{d_{given}} \cdot 8.85 \cdot 10^{-12} \qquad \frac{C_{eq}}{C_{ref}} = 0.111$$

$$Error := 1 - \frac{Re\left(z\left(\frac{-L}{2} + i_{ex} \cdot \pi_{ex}, a, b, K\right)\right)}{Re\left(z\left(\frac{-L}{2}, a, b, K\right)\right)} \qquad Error = 0.01$$

# **Appendix E: Turbo Pascal listing**

This Turbo Pascal program is written and compiled under Borland Pascal version 7.0 calculates by iteration the energetic most ideal charge distribution in a finite square parallel plate capacitor. I confined with giving a simple listing (full of troubles), not answering the actual problem of calculating the capacitance of a perforated plate capacitor. To my opinion this will be more illustrative for further research then a complicated program listing.

```
program charge;
{SA+,B-,D-,E-,F-,G+,I+,L+,N+,O-,P-,Q-,R-,S+,T-,V+,X+,Y+}
{$M 16384,0,655360}
(* Forces must be multiplied by (N^2)/(4*pi*epsilon*side^2)
(* The initial values must be given on the command line.
(* For example: "CHARGE N 6 L 4 U 10" results in the calculation of
(* the situation for two 6*6 partitioned plates with charge 4 on the
(* lower and charge 10 on the upper plate.
(* The air gap is 1 according to the constant definitions
(* The plate are saved as text file in
(* "UP PLATE.DAT" and "LO PLATE.DAT"
uses
        crt,dos;
        maxNN=50;
const
        gap=1;
        side=10;
        error=1;
        charge plate = array[1..maxNN,1..maxNN] of integer;
type
var
        steps:integer;
                                            (* stores the number of iteration steps performed
        NN, init_up, init_lo :integer;
                                            (* store the size and initial values of the configuration *)
        upper plate, lower plate,
                                            (* store the data
        old upper plate,
                                            (* store old data for deciding when to stop
        old lower plate :charge plate;
procedure initialize;
(* Evaluates command line *)
        m,code: integer;
var
begin
  clrscr;
  NN := 5;
  init up := 5;
  init lo := -5;
  if (paramcount=0) or (paramstr(1)='?') then
  begin
   writeln('n xx : matrix size [default 5]');
   writeln('u xx : initial charge upperplate [default 5]');
   writeln('l xx: initial charge lowerplate [default-5]');
   halt(0);
  end:
  for m := 1to parameount do
  begin
   if paramstr(m) = 'n' then val(paramstr(M+1),NN,code);
   if paramstr(m) = 'u' then val(paramstr(M+1),init up,code);
```

```
if paramstr(m) = 'l' then val(paramstr(M+1),init lo,code);
  end;
  writeln('matrix size
                               : ',NN,'*',NN);
  writeln('initial upperplate charge: ',init up);
  writeln('initial lowerplate charge : ',init_lo);
end;
procedure init charge;
(* Fills both plates with uniform initial charge *)
var i,j: integer;
begin
 for i := 1 to NN do
   for j := 1 to NN do
   begin
    upper plate[i,j] := init up;
    lower_plate[i,j] := init_lo;
    old_upper_plate[i,j] := init_up;
    old_lower_plate[i,j] := init_lo;
   end;
end;
procedure Save(plate:charge plate;name:string);
(* Saves array 'plate' to file 'name' *)
var i,j: integer;
   F: text;
begin
  Assign(F, name);
  Rewrite(F);
  for i := 1 to NN do
  begin
    for j := 1 to NN do
    begin
      write(F,plate[i,j]);
      write(F,' ');
    end;
    writeln(F,'');
  end;
  close(F);
end;
function ready: boolean;
(* Decides if ready by watching charge distribution before and after iteration *)
var i,j: integer;
   dummy:boolean;
begin
  dummy := true;
   i:=1; i:=1;
   while dummy and (i<=NN) do
   begin
    while dummy and (j<=NN) do
       dummy := (upper_plate[i,j]=old_upper_plate[i,j]) and
                    (lower_plate[i,j]=old_lower_plate[i,j]);
       inc(j);
    end;
    inc(i);
   end;
   ready := dummy;
   for i := 1 to NN do
```

```
for j := 1 to NN do
   begin
     old_upper_plate[i,j] := upper_plate[i,j];
     old_lower_plate[i,j] := lower_plate[i,j];
   end;
end;
procedure iteration step;
var i,j :integer;
   xforce, yforce :real;
   function allowed(u:integer;f:real): boolean;
    (* checks if an intended move is allowed
    (* this function is to implement more complex structures
   var dum: boolean;
   begin
      dum := ((u=1) \text{ and } (f>0)) \text{ or } ((u=NN) \text{ and } (f<0));
      allowed := (not dum) and (abs(f)>error);
   end;
   function up force(var xforce, yforce:real): boolean;
    (* calculates the force in point i,j of the upper plate
    (* due to all the other charges
   var k,l: integer;
        fact: real;
    begin
      xforce := 0; yforce := 0;
      for k := 1 to NN do
      for 1 := 1 to NN do
      if not ((k=i) and (l=j)) then
      begin
      (* Due to upper plate *)
        fact := (sqr(k-i)+sqr(l-j))*sqrt((sqr(k-i)+sqr(l-j)));
        fact := upper plate[i,j]*upper plate[k,l]/fact;
        xforce := xforce+(k-i)*fact;
        yforce := yforce+(l-j)*fact;
       (* Due to lower plate
        fact := (sqr(k-i)+sqr(l-j))*sqrt((sqr(k-i)+sqr(l-j)+sqr(gap)));
        fact := upper_plate[i,j]*lower_plate[k,l]/fact;
        xforce := xforce+(k-i)*fact;
        yforce := yforce+(l-j)*fact;
      end;
      up_force := (abs(xforce)>error) or (abs(yforce)>error);
   end;
   function lo force(var xforce,yforce:real): boolean;
   (* calculates the force in point i,j of the lower plate *)
    (* due to all the other charges
   var k,l: integer;
        fact:real;
   begin
      xforce := 0; yforce := 0;
      for k := 1 to NN do
        for l := 1 to NN do
          if not ((k = i) \text{ and } (l = j)) then
          begin
        (* Due to upper plate *)
             fact := (sqr(k-i)+sqr(l-j))*sqrt((sqr(k-i)+sqr(l-j)+sqr(gap)));
             fact := lower plate[i,j]*upper plate[k,l]/fact;
```

```
xforce := xforce+(k-i)*fact;
            yforce := yforce+(l-j)*fact;
        (* Due to lower plate *)
            fact := (sqr(k-i)+sqr(l-j))*sqrt((sqr(k-i)+sqr(l-j)));
            fact := lower_plate[i,j]*lower_plate[k,l]/fact;
            xforce := xforce+(k-i)*fact;
            yforce := yforce+(l-j)*fact;
         end:
         lo force := (abs(xforce) > error) or (abs(yforce) > error);
   end;
   procedure move charge(xf,yf: real; var plate: charge plate);
   var delta_x, delta_y: integer;
   begin
      delta_x := 0; delta_y := 0;
      if allowed(i,xf) then
       begin
         if (xf > 0) then delta_x := 1;
         if (xf < 0) then delta_x := -1;
       if allowed(j,yf) then
       begin
        if (yf > 0) then delta y := 1;
         if (yf < 0) then delta_y := -1;
      if abs(delta_x) + abs(delta_y) \Leftrightarrow 0 then
      begin
        plate[i,j] := plate[i,j]-1;
        plate[i-delta_x,j-delta_y] := plate[i-delta_x,j-delta_y]+1;
      end;
   end;
begin
  for i := 1 to NN do
   for i := 1 to NN do
   begin
    (* upper plate *)
      if up force(xforce,yforce) then move charge(xforce,yforce,upper plate);
    (* lower plate
      if lo_force(xforce,yforce) then move_charge(xforce,yforce,lower_plate);
   end;
end;
begin
 initialize;
 init charge;
 steps := 0;
 repeat
  iteration_step;
  inc(steps);
  gotoxy(1,5);
  writeln('Iteration step: ',steps);
 until ready;
 writeln;
 save(upper plate, 'UP PLATE.DAT');
 writeln('Upper plate saved as: ,"UP PLATE.DAT"');
 save(lower plate,'LO PLATE.DAT');
 writeln('Lower plate saved as:, "LO PLATE.DAT"');
end.
```

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